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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/833,953	04/11/2001	Marco Racanelli	00CON161P	3823

7590 03/07/2002

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EXAMINER
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MALDONADO, JULIO J

ART UNIT	PAPER NUMBER
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2823

DATE MAILED: 03/07/2002

# 2

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/833,953

Applicant(s)

RACANELLI, MARCO

Examiner

Julio J. Maldonado

Art Unit

2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☐ Responsive to communication(s) filed on 11 April 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☐ Claim(s) 1-25 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☐ Claim(s) 1-25 is/are rejected.
- 7) ☐ Claim(s) 1, 9, 12, 20 and 23 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other.

## DETAILED ACTION

### *Claim Objections*

1. Claims 1, 9, 12, 20 and 23 objected to because of the following informalities: in claim 1 says "...forming a transistor gate and a field oxide region; doping with a first dopant said layer over said transistor gate \_\_\_ without..." should say "...forming a transistor gate and a field oxide regions; doping with a first dopant said layer over said transistor gate regions without...". In claims 9 and 20 says "...approximately  $6.5 \times 10^{15}$ ..." should say "...approximately  $6.5 \times 10^{15}$ ...". In claims 12 and 23 says "...approximately  $1.0 \times 10^{15}$ ..." should say "...approximately  $1.0 \times 10^{15}$ ...". Appropriate correction is required.

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 3, 6-12, 14-23 rejected under 35 U.S.C. 102(b) as being anticipated by Zaccherini (U.S. 5,436,177).

In reference to claim 1 and 14 Zaccherini (Fig.1-6) teaches an analogous method to form implanted regions including the steps of forming a layer (7) comprising polycrystalline silicon over a transistor gate (4) and a field oxide (5) regions; forming a doping barrier (10) above said polycrystalline silicon; doping with a first dopant (11) said

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layer over said transistor gate without doping said layer over said field oxide region (5); removing said doping barrier (10); doping said layer over said transistor gate (4) and said field oxide regions (5) with a second dopant (13) so as to form a resistor in said layer (7) over said field oxide region (5).

In reference to claim 3, 6-12 and 15-23 Zaccherini teaches that said layer (7) comprises polysilicon; that said field oxide (5) comprises silicon oxide; that first dopant (11) is an N-type dopant comprising phosphorous at a dose of approximately  $6.5 \times 10^{15}$  atoms per square centimeter; that the second dopant is a P-type dopant comprising boron at a dose of approximately  $1.0 \times 10^{15}$  atoms per square centimeter; and that said doping barrier (10) comprises a photoresist; that the polycrystalline silicon layer includes a gate region (4).

### ***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claim 2, 4-5, 13 and 24-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zaccherini ('177) in view Liu et al. (U.S. 6,165,861).

In reference to claims 2, 4-5, 13 and 24-25 Zaccherini teaches all aspects of the invention but fails to teach the formation of a contact region for said resistor comprising a silicide. Nevertheless, Liu et al. (Fig.7) teaches in an analogous method for forming integrated resistors including a contact region comprising a titanium silicide (20).

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Furthermore, Liu et al. teaches that the transistor gate can be a gate of a PFET or a gate of a NFET (column 4, lines 11-24).

Therefore, it would have been obvious to one of basic skill in the art to combine the teachings of Zaccherini and Liu et al. to arrive the claimed invention. The motivation/suggestion would be to make interconnections to other levels within the circuit and providing shielding of the resistor during subsequent processing (column 4, lines 25-41). Furthermore, it would have been obvious to one skilled in the art that by using additional masking steps, both PFET and NFET can be made into the substrate (column 4, lines 11-24).

### ***Conclusion***

5. Papers related to this application may be submitted directly to Art Unit 2823 by facsimile transmission. Papers should be faxed to Art Unit 2823 via the Art Unit 2823 Fax Center located in Crystal Plaza 4, room 3C23. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2823 Fax Center number is **(703) 305-3432**. The Art Unit 2823 Fax Center is to be used only for papers related to Art Unit 2823 applications.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Julio J. Maldonado** at **(703) 306-0098** and between the hours of 8:00 AM to 4:00 PM (Eastern Standard Time) Monday through Friday or by e-mail via [julio.maldonado@uspto.gov](mailto:julio.maldonado@uspto.gov). If attempts to reach the examiner by telephone

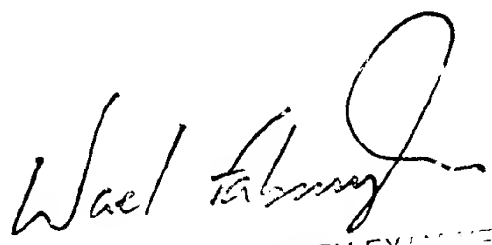
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are unsuccessful, the examiner's supervisor, Wael Fahmy, can be reached on (703) 308-4918.

7. Any inquiry of a general nature or relating to the status of this application should be directed to the **Group 2800 Receptionist** at (703) 308-0956.

8. The following list is the Examiner's field of search for the present Office Action:

U.S. Class / Subclass(es): 438/382, 438/385	02/25/2002
Other Documentation:	
Electronic Database(s): EAST (USPAT, US-PGPUB, EPO, JPO, DERWENT, IBM)	02/25/2002

  
SUPERVISOR/PRIMARY EXAMINER  
TECHNOLOGY CENTER

**Julio J. Maldonado**

Patent Examiner

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